Miniaturized Reverse Modulation Loop of a CQPSK 120-Mbit/s Modem for Spacecraft Applications

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Abstract—**The design and performance of a miniaturized reverse modulation loop (RML) for a 120-Mbit/s coherent quadrature phase shift keying (CQPSK) modem for on-board satellite applications are presented. Analysis of time delays within the RML circuit indicates that any differential time-delay errors can adversely affect the associated BER and should be minimized. The RML circuit, consisting of a modulator, demodulator, and comparator circuit, has been fabricated using quasi-monolithic techniques with dimensions of 1.65 × 4 cm. The relative phase for all four states of the modulator is in close agreement with design values of 90° ± 1° over a 200-MHz bandwidth at 3.95 GHz. The demodulator and comparator circuits of the RML have successfully recovered a 120-Mbit/s bit stream. The RML circuit is capable of recovering higher bit rates because of relatively uniform amplitude and phase performance over the 3.7- to 4.2-GHz communications satellite band.**

Introduction

FUTURE communications satellite configurations are envisioned to include multibeam phased-array antennas, on-board signal regeneration, and switching at baseband and microwave frequencies [1]. On-board demodulation and remodulation of digitally modulated signals in communications satellites offer substantial link-budget advantages because of the separation of up-link and down-link bit error rate (BER) performance characteristics [2]. Coherent quadrature phase shift keying (CQPSK) modems, which require carrier recovery on board the satellite, offer a potential 2.5-dB performance advantage over differential detection schemes [3]. This advantage may be used to improve transmission quality, reduce earth station size, increase the data throughput rate, or reduce the satellite's effective isotropically radiated power (e.i.r.p.). A second advantage of coherent systems is the avoidance of one-symbol time delays (16.6 ns in a 120-Mbit/s system) [4]. However, additional hardware, in the form of a very stable voltage-controlled oscillator (VCO), is necessary for carrier recovery in a CQPSK repeater [4], [5]. One of the key requirements for on-board satellite application of CQPSK modem technology is the development of light-weight reverse modulation loop, power-efficient hardware with high reliability.

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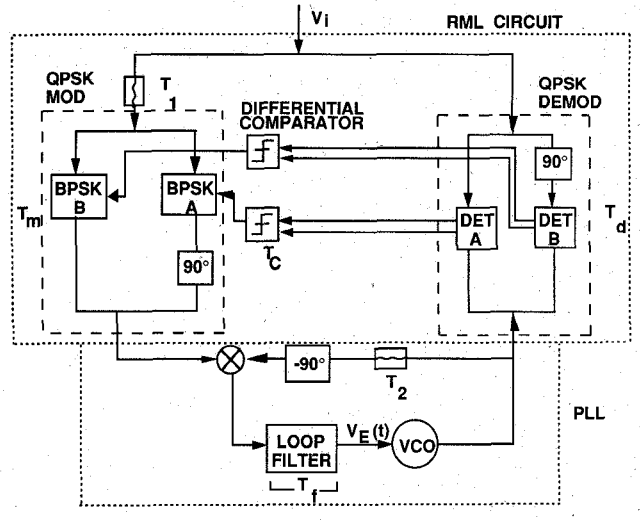

Fig. 1. Reverse modulation loop system showing time delays.

The reverse modulation loop (RML) method of implementing the carrier recovery portion of a CQPSK modem (Fig. 1) uses less hardware than the fourth-power method [5] and the Costas Loop [6] approach. The fourth-power method requires coherent frequency translation for narrowband filtering and RF amplification [5], thus using more hardware than the RML. The Costas Loop requires even additional hardware because the incoming signal is split and multiplied by the carrier and a carrier in quadrature [6]. The resulting signals are band-limited, multiplied together, and summed to produce an error signal to the VCO for carrier recovery.

An added advantage of an RML design is that the circuit can be fabricated using quasi- or fully monolithic microwave integrated circuit (MMIC) technology, resulting in decreased size and increased reliability. In addition, the RML design demodulates the data as part of the carrier recovery process. However, analysis has shown that the time delays [7] in the RML circuit are very critical, and any errors in the time delays can adversely affect the associated BER and the rate of cycle slippage [8]. The absolute delays through the RML can be compensated and do not adversely affect the loop parameters discussed above. Longer delay line lengths are expected to produce larger errors because of line length uncertainties and variations due to temperature. Therefore, these RF delays

should be reduced by circuit miniaturization and by minimizing baseband delays.

This paper presents the design and performance of a miniaturized RML circuit for carrier and data recovery in a 120-Mbit/s modem. Key features of this circuit include significant size reduction and reliability enhancement by monolithic integration of resistors and capacitors on an alumina substrate, and performance enhancement by minimizing time delays in the RF and the comparator circuits.

RML Circuit and Time Delays

The three basic sections of an RML circuit are the demodulator, the comparator, and the modulator, as shown in the block diagram in Fig. 1. The demodulator is used to recover in-phase and quadrature (I and Q) bit streams. These data are then hard-limited and inverted by a digital comparator. The data are used to modulate the delayed modulated signal from which they were recovered, yielding the carrier. The correct operation of this system depends on synchronizing the modulated carrier, the data, and a locally generated carrier by using an additional phase-locked loop (PLL). All the internal circuit delays (e.g. T_c, T_d, T_m, etc.) and external compensating time delay elements (e.g. T_1 and T_2) are shown in the circuit block diagram. Static analysis of time delays [7]–[9] shows that delay line T_1 must be designed to compensate for the delays of the detector and comparator (T_d, and T_c), so that

$$T_1 = T_d + T_c. \tag{1}$$

The detector delays are relatively small and may be further reduced by circuit miniaturization. The comparator circuit delay at baseband contributes significantly to the RF delay line length and must be reduced by using faster devices. Thus the static delays can be reduced and also compensated by appropriate design choices. Therefore, these delays do not degrade the (BER) performance.

The differential delays, however, will introduce an extra phase term $\Delta\Phi_D = \omega_c(T_1 + T_m - T_2)$ in the recovered carrier of the PLL. Using Sherman's method [10], it can be shown [8] that the probability of single-bit errors (P_{b1}) as a function of differential time delay errors may be expressed as

$$P_{b1} = \frac{1}{4}\left[\operatorname{erfc}\left(\sqrt{\frac{2E_b}{N_o}}\cos\left\{\Delta\Phi_D + \frac{\pi}{4}\right\}\right) + \operatorname{erfc}\left(\sqrt{\frac{2E_b}{N_o}}\sin\left\{\Delta\Phi_D + \frac{\pi}{4}\right\}\right)\right] \tag{2}$$

where erfc is the complementary error function, E_b/N_o is the energy-per-bit to noise-density ratio, and $\Delta\Phi_D$ is the differential time delay error.

Fig. 2 shows P_{b1} versus E_b/N_o for different values of $\Delta\Phi_D$. A 2° time delay phase error requires less than 0.15 dB additional E_b/N_o to achieve the same error performance, compared with the ideal case ($\Delta\Phi_D = 0$) for a probability of error of 10^{-6}. In contrast a 4° phase error requires a 0.4 dB higher signal-to-noise ratio to achieve this performance. The sensitivity of BER performance to differential phase error highlights the importance of restricting time delay and equivalent phase variations. Of particular importance are the $\Delta\Phi_D$ variations as a function of temperature and their impact on the modem performance.

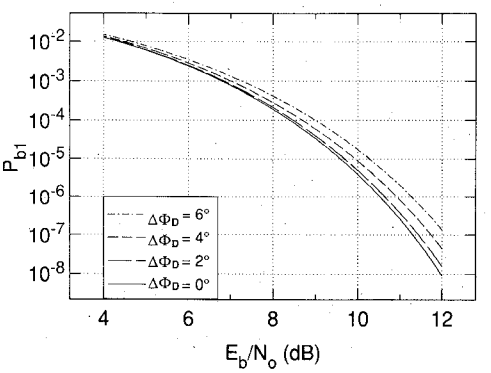

Fig. 2. Probability of bit errors versus E_b/N_o for differential phase errors.

Hardware Design and Fabrication

Fig. 3(a) is a block diagram of the demodulator. The carrier enters the demodulator through a Wilkinson divider and is split evenly between two detectors. Similarly, the modulated carrier is split by the 3-dB quadrature hybrid and enters the other detector port. The detector (Fig. 3b) uses diode mixers and low-pass filters to extract data from the modulated carrier. The mixer design uses a pair of forward-biased Schottky diodes and a quadrature hybrid. Each detector has two complementary outputs, which are passed through low-pass filters and reshaped by the comparator circuit. The filters also function as bias lines for the diodes, eliminating the need for an extra bias network. The low-pass filter, implemented with an inductance capacitance (LC) network, is designed with a cutoff frequency of 1 GHz and a flat group delay. The filter provides greater than 30-dB rejection for frequencies greater than 2 GHz.

The circuits were designed and modeled using the SuperCompact™ and Touchstone™ computer-aided-design (CAD) packages. Appropriate changes were made to the computer model to include discontinuities such as bends and junctions, as well as coupling between the lines. Wherever possible, narrow transmission lines with higher inductance per unit length and smaller line spacing were used to make the circuit compact. The circuits were designed to be highly symmetrical in order to reduce the effects of noise and minimize the effects of fabrication tolerances.

The comparator circuit consists of a gallium arsenide (GaAs) integrated circuit (IC) chip and an alumina substrate with printed lines and resistors for the required inputs and outputs. A dual differential amplifier was se-

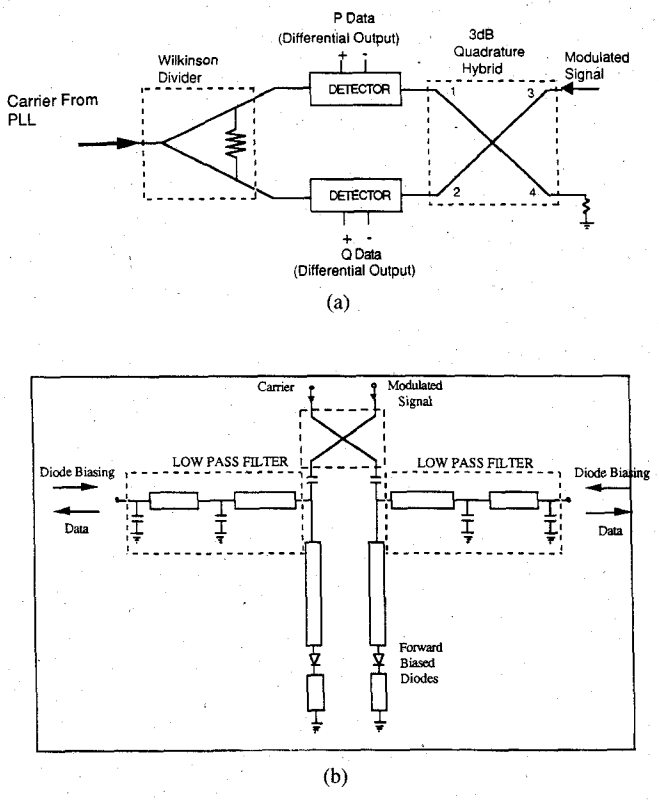

Fig. 3. Circuit diagram of the RML demodulator. (a) Demodulator circuit. (b) Detector.

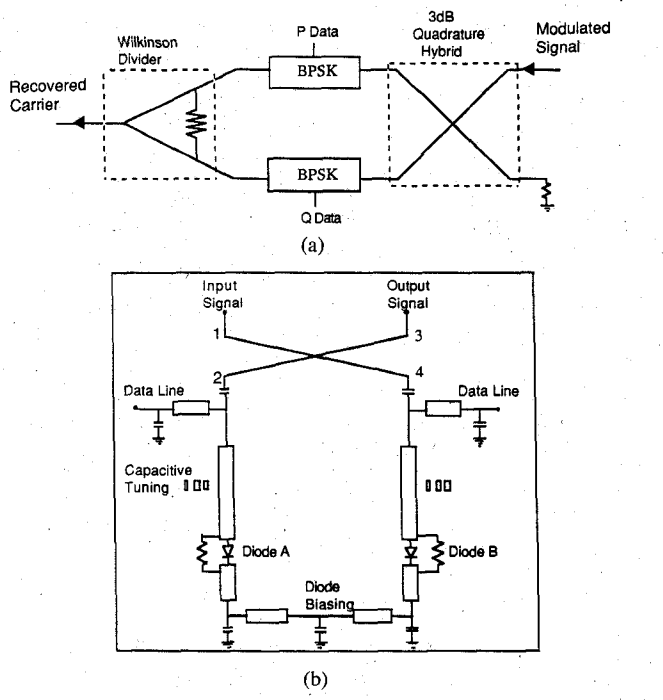

Fig. 4. Circuit diagram of the RML modulator. (a) Modulator circuit. (b) BPSK element.

lected for comparator applications. This IC is designed to operate at frequencies up to 1.75 GHz with an average propagation delay of 375 ps. The 1.30 × 1.75-mm chip is mounted in die form to minimize the overall circuit size. The propagation delay through the comparator circuit must be compensated by RF delays in the RML circuit. The comparator delay of 0.375 ns results in a significant reduction in the size of the delay lines and the modem.

A resistive network, which can be adjusted in discrete increments at the differential amplifier input provides the dc bias for the demodulator diodes. These diodes require a bias between 0.20 and 0.45 V to operate in the square law region. At the comparator output, pull-up resistors provide a termination for the open emitter of the amplifiers, and the series resistors act as current limiters to protect the modulator circuit. Only one comparator output is used for switching the modulator; the second may be used in the modem clock recovery circuit. The variable threshold control resistor network allows the threshold switching voltage to be adjusted for interfacing to emitter coupled logic (ECL) voltage levels. Both the threshold voltage and the dc bias for the demodulator diodes should be identical for good common mode rejection of incoming signals. Large, discrete shunt capacitors connected between the power supply voltages and ground prevent transient voltage spikes from interfering with the data.

The modulator (Fig. 4(a)) uses a quadrature hybrid to split the incoming signal into two signals 90° out of phase. Each signal is modulated in a binary phase shift keying (BPSK) circuit with the I and Q data streams from the comparator. The two BPSK outputs are then recombined by an in-phase Wilkinson divider to yield the carrier. The BPSK circuit (Fig. 4(b)) is a reflection-type design with diodes acting as virtual shorts or opens to give the required phase shift between states. A resistor network parallel to each diode is designed to compensate for the finite on-state resistance of the Schottky diodes and provide the desired amplitude balance between the states. The Schottky diode has a forward resistance of ~15 Ω, which corresponds to a reflection loss of approximately 2.7 dB. Schottky diodes are preferable to p-i-n diodes in this design because of their small control signal power, simpler design, and faster switching time. The data lines, dc blocking capacitors, and diode control lines were included in the LC phase-matching network used to compensate for the finite package reactance of the diodes and to provide the necessary 180° phase shift between states.

Fig. 5 is a photograph of the RML circuit, which has overall dimensions of 1.65 × 4 cm. The circuit was reduced in size by using a quasi-monolithic approach in which the passive elements are deposited on a substrate using MMIC fabrication techniques, and discrete active devices are then selected and mounted in the circuit. In addition, thin-film resistors and metal-insulator-metal (MIM) capacitors were used wherever possible to make the layout compact. Air bridges were used in the quadrature hybrids instead of bondwires. A substrate height of 15 mil was selected to allow wider lines for the quadrature hybrid design in order to minimize losses. Realization of the RML circuit on a single substrate, and reduction of the number of discrete components, should increase circuit reliability while reducing the length of interconnection lines and circuit assembly time.

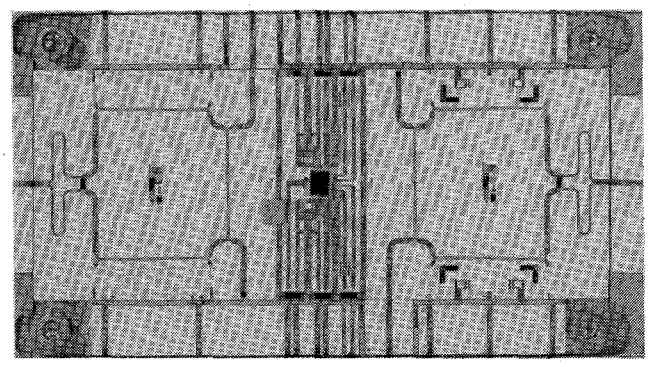

Fig. 5. The reverse modulation loop (dimensions: 1.65 × 4 cm).

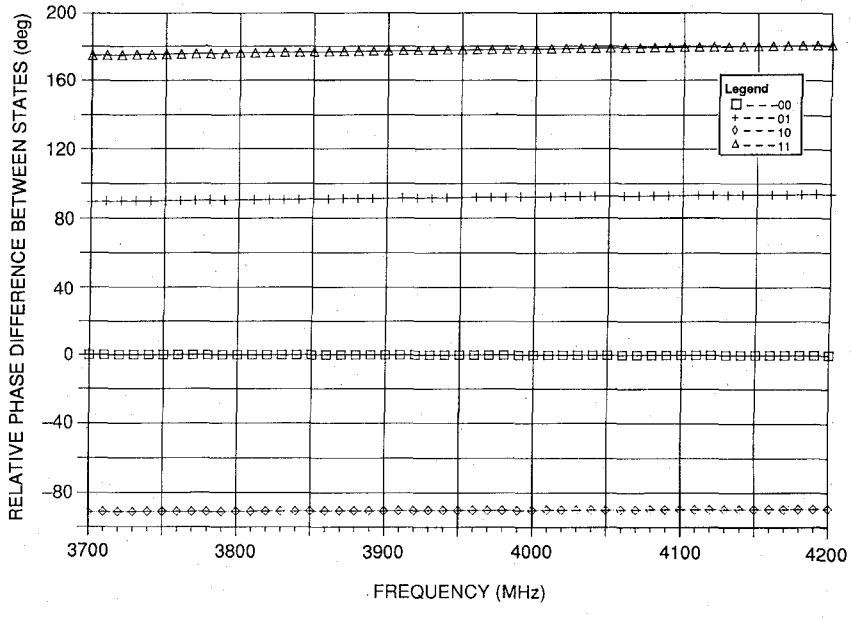

Fig. 6. Measured phase difference between modulator states.

Measured Results

The three sections of the RML were tested individually using an aluminum test fixture designed to test the performance of the RML circuit components. The RML circuit was epoxied to a Kovar test carrier which can be mounted in the test fixture, allowing it to be reused for the final modem assembly. A metal ridge was used on the carrier to provide ground connections for the entire circuit. Alumina distribution boards were employed so that the circuit could easily be assembled and removed from the test fixture.

The modulator was tested in the static mode with an HP8510 network analyzer system for amplitude and phase balance. The measured relative phase difference between the four modulator states was in close agreement with modeled values of 90° ± 1° over a 200-MHz bandwidth at 3.95-GHz center frequency. The relative phase performance is quite uniform over the full 500 MHz bandwidth (Fig. 6) making the circuit useful for wider band applications. The average modulator insertion loss (Fig. 7) was 8.4 dB, which was 0.8 dB higher than the predicted values. This could be caused by fixture and RF connector losses. The amplitude balance was within ±0.3 dB, and the input and output return losses were better than 20 dB across the frequency band of operation. Dynamic measurements of the modulator were performed by mixing the output of the modulator with a carrier and observing the resulting data on an oscilloscope. The modulator rise time of 1.4 ns was measured by observing the transient response for a single bit, making it possible to operate the modulator at bit rates higher than 120 Mbit/s.

Measurements were made on the demodulator to determine the phase balance between all four states. For these measurements, the detected outputs were applied to horizontal and vertical traces of an oscilloscope. To check the demodulator's response during state transitions, a low-speed (8-kHz) random bit pattern was modulated on a carrier and detected with the demodulator. As shown in Fig. 8, the transitions between the four phase states (represented by the lines between the corner points) are clean. The blurring at the corners represents a return to the same

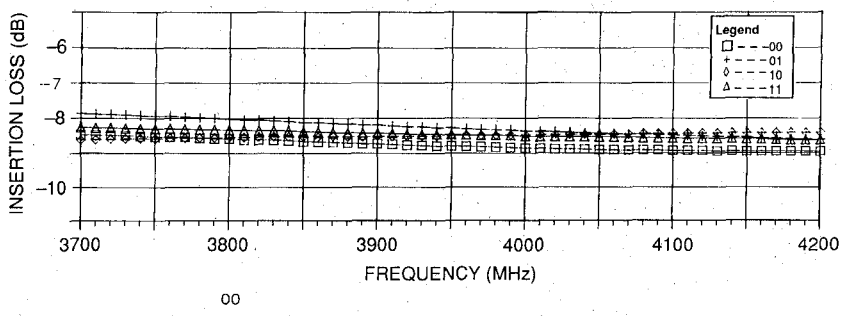

Fig. 7. Insertion loss for modulator states.

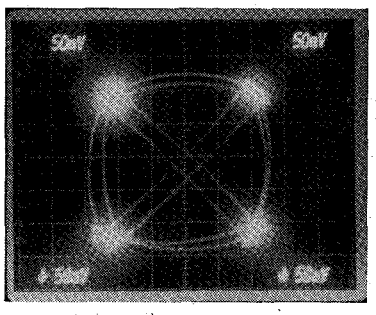

Fig. 8. Phase balance and transient response of the demodulator.

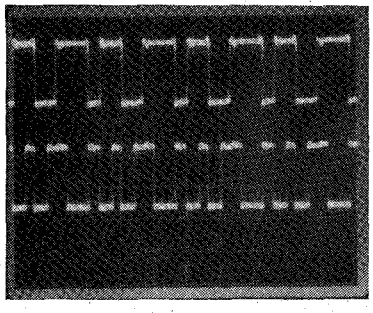

Fig. 10. Comparator outputs for different data patterns.

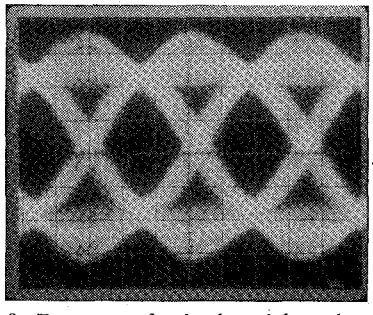

Fig. 9. Eye pattern for the demodulator detector.

state in successive bits, and the associated transients. The eye pattern shown in Fig. 9 was generated for each detector by viewing the detected data on an oscilloscope for a random $2^{23} - 1$ bit pattern. The resulting steady-state pattern also shows smooth transitions between states, an open eye shape, and focused data points.

The comparator circuit was independently tested by simulating the input from the demodulator with a pulse generator. These tests showed that the circuit could be operated well with input levels of 100 mV. The comparator circuit was also tested with detected signals from the demodulator as its inputs. The demodulator produced an output level of 25 to 75 mV into a 50-Ω load. The comparator pull-up resistors used for biasing the detector diodes and the threshold resistor were adjusted for a diode bias voltage of 0.45 V to maximize the demodulated data amplitude. The comparator outputs for both I and Q data streams were then observed for several 16-bit words, as shown in Fig. 10. For modulated signal and clean carrier power levels of 1.8 and 1.2 dBm, respectively, the comparator output voltage was 0.5 V for a detected bit.

Conclusions

A miniaturized RML circuit, which consists of demodulator, comparator, and modulator circuits, has been designed and fabricated using a quasi-monolithic approach on a single substrate. The amplitude and phase balance of the modulator closely approach the design goals. The demodulator and comparator were demonstrated to successfully recover data at 120 Mbit/s. These results show that the RML circuit components are capable of being integrated into a miniaturized 120-Mbit/s CQPSK modem. Use of a quasi-monolithic approach increases circuit reliability while reducing the number of discrete components and the circuit assembly time. Reduction in time delay errors due to shorter interconnect lines results in BER performance improved.

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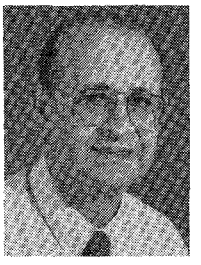
Dr. Gupta has served as Vice-Chairman (1987–88) and Chairman (1988–89) of the Washington DC/Northern Virginia Chapter of the IEEE MTT Society. He has authored/coauthored more than 45 papers on solid-state devices and circuits, GaAs MMIC's, advanced microwave subsystems and satellite systems. He holds two patents and is a co-recipient of the best paper award for the 8th International Conference on Digital Satellite Communications (ICDSC-8). He serves on the Editorial Board of *COMSAT Technical Review*.



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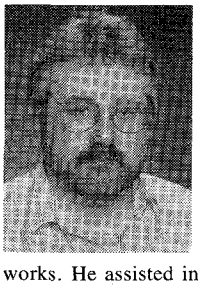
Mr. Assal holds patents in communications satellite configurations and hardware. In 1982 he received the COMSAT Laboratories Research Award. He is a member of Tau Beta Pi and Eta Kappa Nu.



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